31.3 An 802.11a/b/g RF Transceiver in an SoC

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The emerging mass market of cellular terminals with integrated WLAN systems demands for high-performance low-power low-cost SoCs that can operate in all WLAN frequency bands. Low out-of-band transmitter radiation and high receiver linearity are required to avoid interference since all wireless systems can be active simultaneously with antenna isolation of only 15dB. The 802.11a/b/g SoC described in this paper fulfills these requirements and as shown in Fig. 31.3.1 includes the following blocks: RF transceiver with fully calibrated transmitter, PHY, power-management, MAC, memory, and digital interface. The SoC is used in a commercially available front-end module with power amplifier and RX/TX switch.

A direct-conversion architecture with broadband 12GHz VCO and a divide-by-2 frequency divider instead of dual-conversion architecture [1] has been chosen to reduce intermodulation products and spurious emissions that fall into the receive band of the coexistent cellular system (Fig. 31.3.2).

In the transmitter, a highly-linear low-current 2.5V TX mixer circuitry with a power efficient PGA operates at 1.5V supply voltage. High power efficiency of the transmit path is achieved by low output power backoff to saturation. The IEEE 802.11a/g specification regarding EVM can be fulfilled with a backoff of 5.5dB, when the compression characteristic of the transmitter follows an ideal limiter function [3]. The distortion in the vector modulator is mainly created by the differential amplifier of the Gilbert mixer. An opamp with resistive feedback controls the differental amplifier and suppresses the harmonics of the baseband signal (Fig. 31.3.3). The vector modulator with opamp and biasing circuit draws 8mA while delivering -12dBm output power. In deep submicron CMOS technology the distortion of the PGA is mainly determined by the velocity saturation and electron mobility of the transistors. The linear range of the PGA transistors is exploited by appropriate adjustments in transistor gain, bias current, and load impedance of the amplifier.

A separate downconversion mixer is used to measure the image sideband and the carrier feedthrough of the transmitter while a sinusoidal test signal is injected at the baseband input for calibration after power-up. The I/Q impairments are adjusted by a digital offset and phase shift in the baseband signal after a spectral analysis of the mixer output signal on the chip.

The load of the differential TX PGA is an integrated coil with center tap for DC feed which is unsymmetrically connected via a capacitor to the single-ended power amplifier of the front-end module (Fig. 31.3.4). The 50Ω output impedance of the transmitter is well defined over a broad frequency range by the inductance of the coil. An expensive external TX-balun with matching components is not required.

The TX output power control with a dynamic range of 30dB and a resolution of 1dB is distributed between the mixer and the PGA. The gain in the PGA is switched by the cascode transistors of 32 differential RF amplifiers reducing the current draw by 50% with each 6dB step. Only 5 fine steps of 1dB resolution are needed to switch the mixer feedback resistance resulting in a low carrier feedthrough due to the low offset voltage at low output power.

The fully differential receiver is built up with an integrated common source LNA operated at 1.5V. High linearity and selectivity are achieved by using inductive source degeneration and the inductive load in the narrowband 2.4GHz band. The low-Q inductance of the high band serves for broadband frequency characteristic. The LNA incorporates a 23dB gain step to cover the whole dynamic range. The switching quadrature transistors in the Gilbert mixer of the downconverter are driven by hard switching rail-to-rail LO buffers to avoid flicker noise [4]. An RSSI monitors the receiver input level. The gain of the LNA and demodulator is 33dB with a noise figure of 3.5dB in the low band and 4dB in the high band.

The VCO has to cover all WLAN frequency bands with two cores working between 4.8 and 5GHz, and 9.8 and 11.8GHz, respectively. It is a digitally controlled LC-VCO using a switched-capacitor bank, an NMOS transistor core and PMOS varactors. This fulfills pushing and constant K_{VCO} requirements over the band. The measured phase noise at 1MHz distance from the carrier is –120dBc/Hz and –115dBc/Hz for the low and high band, respectively, over the whole frequency band.

The crystal oscillator provides a reference signal at 40MHz using an 11pF crystal. The structure is that of a Colpitts oscillator with a switched capacitor bank, ensuring ±60ppm frequency adjustment range. Current boosting is used at the start up. The measured phase-noise is -135dBc/Hz at 1kHz offset from the carrier. An external reference signal can be fed into the PLL supporting reference frequencies from 19.2 to 100MHz.

The type-I ΔΣ-PLL with 3rd-order MASH modulator has a linear charge pump with offset current. The bandwidth of the integrated 5th-order loop filter is 200kHz and ensures low reference spurious signals. The open loop gain of the PLL is automatically calibrated after programming the VCO frequency via a 3-wire bus [5].

The generation of quadrature LO signals is done by a differential CML master-slave structure with ac-coupling and high ohmic pre-biasing at the clock inputs to enable good performance over temperature, process, and frequency. This structure requires about 10mA for 802.11a and 4mA for the 802.11b/g modes.

The cut-off frequency of the 5th-order ladder-type butterworth baseband filter can be programmed to 7, 14, 20, and 40MHz. Therefore, the system not only covers the current WLAN standards, it also compatible with the larger bandwidth requirements of the upcoming 802.11n standard. The capacitors are digitally tunable to compensate for process variations.

Due to the high filter attenuation in the alternate channel the DAC and ADC can be operated at double Nyquist rate of 40MHz. This allows for low overall power consumption. The measurement results show that the P_{1dB} is 1.3dB below the saturated output power of 8.5dBm (Fig. 31.3.5). The measured transmitter output power is –2.5dBm and –2dBm at 2.4 and 5GHz outputs with an EVM of –32dB and –31dB, respectively. The output power drop is 1dB over the whole frequency range from 4.9 to 5.8GHz. The sensitivity of the receiver is –77 and –74dBm referred to the LNA input.

The SoC is produced in a 1P6M 0.13μm CMOS technology with MIM-caps of 2fF/μm² sheet capacitance. The SoC is housed in a 169-pin BGA package. Figure 31.1.6 shows a die micrograph of the RF macro with a chip size of 6.7mm² including the on-chip voltage regulators.

References:

[1] L. Nathawad, D. Weber, S. Abdollahi, et al., "An IEEE 802.11 a/b/g SoC for Embedded WLAN Applications," *ISSCC Dig. Tech. Papers*, pp. 364-365, Feb., 2006.

[2] O. Charlon et al., "A Low-Power High-Performance SiGe BiCMOS 802.11a/b/g Transceiver IC for Cellular and Bluetooth Co-Existence Applications," *IEEE J. Solid-State Circuits*, vol.41, pp.1503-1512, July, 2006.

[3] W.J. McFarland, "WLAN System Trends and the Implications for WLAN RFICs," *IEEE RFIC Symp. Dig. Papers*, pp. 141-144, June, 2004.

[4] H.Darabi and A. Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model," *IEEE J. Solid-State Circuits*, vol. 35, no.1, pp. 15-25, Jan., 2000.

[5] E. Götz, H. Kröbel, G. Märzinger, et al., "A Quad-Band Low Power Single Chip Direct Conversion CMOS Transceiver with ΔΣ-Modulation Loop for GSM," *Proc. ESSCIRC*, pp. 217-220, Sep., 2003.

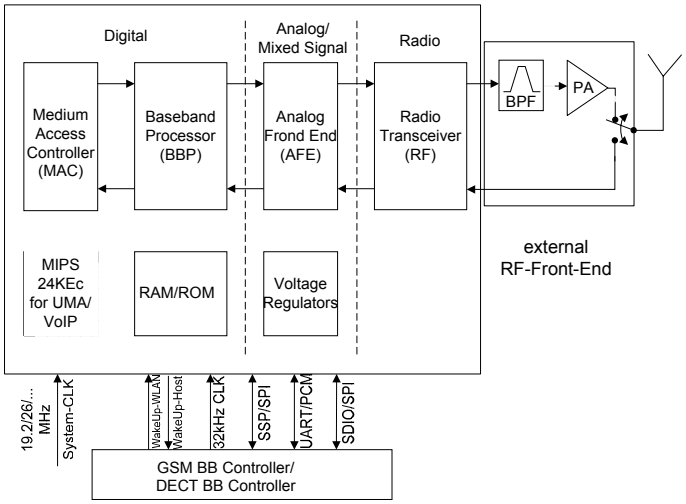

Figure 31.3.1: Block diagram of the 802.11a/b/g SoC.

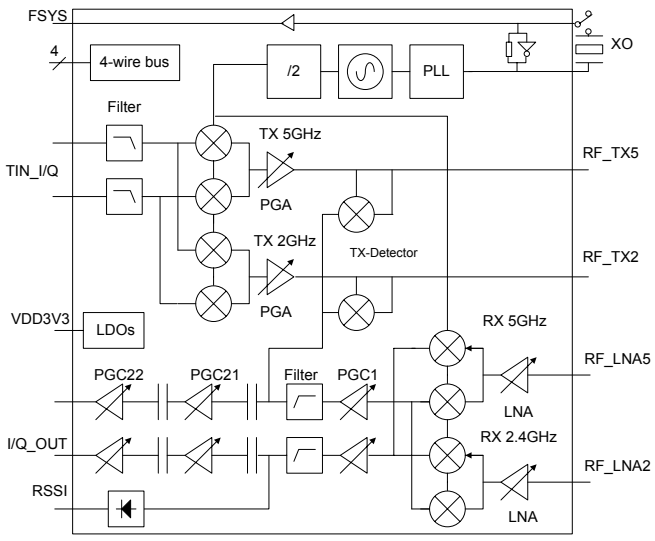

Figure 31.1.2: Block diagram of the RF Transceiver.

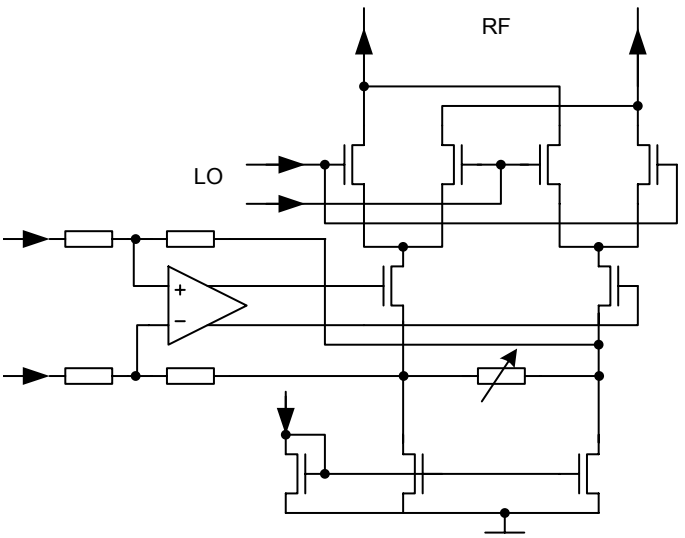

Figure 31.3.3: Simplified schematic of the TX mixer.

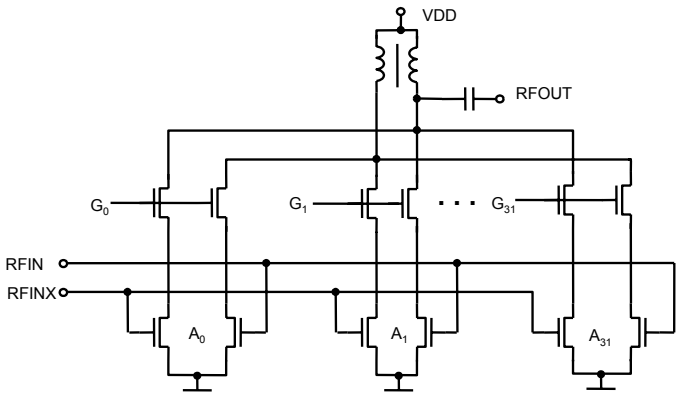

Figure 31.3.4: Simplified schematic of the TX RF PGA.

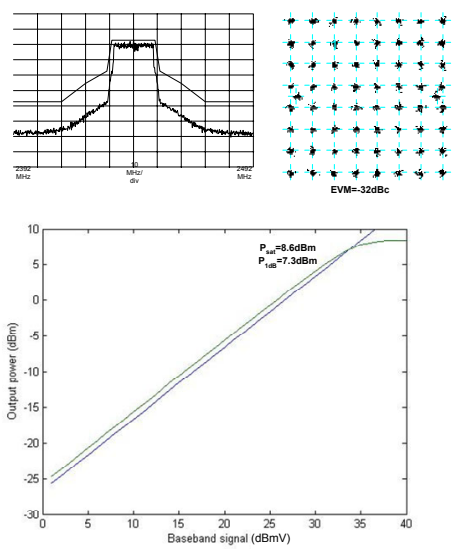

Figure 31.3.5: TX measurement results.

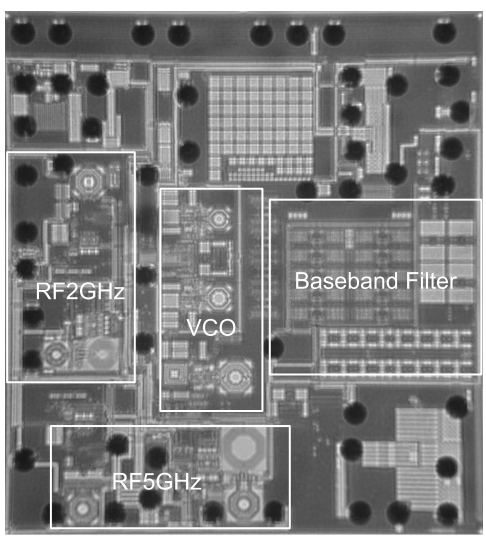

Figure 31.3.6: Micrograph of the SoC RF macro.

Continued on Page 622

Parameter	2.4 GHz Band	5 GHz Band
Transmit EVM	−32dB@ −2.5dBm	−31dB@ −2dBm
Spurious emissions (except harmonics)	< −65dBc	< −65dBc
Receiver Sensitivity at 54Mb/s	−77dBm	−74dBm
RX P_{1dB} Compression point (high/low gain)	−22/ −5dBm	−21/ −4dBm
Receiver Noise Figure	3.5dB	4.0dB
Phase Noise @1MHz offset	−120dBc/Hz	−115dBc/Hz
TX current consumption (excl. DAC)	@1.5V @2.5V 56mA 27mA	@1.5V @2.5V 65mA 39mA
RX current consumption (excl. ADC)	@1.5V @2.5V 44mA 25mA	@1.5V @2.5V 49mA 31mA
Technology	1P6M 0.13µm CMOS with MIMCAP option	
Package of SoC	169 Flip-Chip BGA	
Power down leakage power	< 30µW	

Figure 31.3.7: Measurement results.

